WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a reference potential conversion circuit which is supplied with n-1 (n is 2 or larger natural number) external reference potentials (VREF1, VREF2, ..., VREFn-1) and converts external reference potentials to generate n-1 internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) differing from external reference potentials and having a relationship with regard to the n-1 external reference potentials, and

an input circuit which is supplied with said internal reference potential (VREFint1, VREFint2, ..., VREFintn-1) as reference potentials, is supplied with n values of data signals expressed by potentials, and compares a data signal and a reference potential to output a determination result.

2. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1)is expressed by VREFintn-1 = VREFn-1 + A (n is 2 or larger natural number and A is a rational number except 0).

3. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials

(VREFint1, VREFint2, ..., VREFintn-1) is expressed by VREFintn-1 = B × VREFn-1 (n is 2 or larger natural number and B is a rational number except 0).

4. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is expressed by VREFintn-1 = C × VREFn-1 + D (n is 2 or larger natural number and, C and D are rational numbers except 0).

5. The semiconductor integrated circuit according to claim 1, further comprising a storage circuit for holding data of a plurality of bits, and wherein

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said storage circuit.

6. The semiconductor integrated circuit according to claim 5, wherein

said storage circuit for holding data of a plurality of bits is a one-time programmable storage circuit, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of

bits stored in said storage circuit.

7. The semiconductor integrated circuit according to claim 6, wherein

said storage circuit includes a laser beam blown type fuse for specifying data of a plurality of bits to be held depending on whether a laser beam disconnects the fuse, and wherein

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said laser beam blown type fuse.

8. The semiconductor integrated circuit according to claim 6, wherein

said storage circuit includes an electric current blown type fuse for specifying data of a plurality of bits to be held depending on whether an electric current disconnects the fuse, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said electric current blown type fuse.

9. The semiconductor integrated circuit according to claim 6, wherein

said storage circuit includes a dielectric film breakdown type fuse for specifying data of a plurality

of bits to be held depending on whether a voltage breakdowns a dielectric film of the dielectric film breakdown type fuse, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said dielectric film breakdown type fuse.

10. The semiconductor integrated circuit according to claim 5, wherein

said storage circuit for holding data of a plurality of bits is a reprogrammable storage circuit, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said storage circuit.

11. The semiconductor integrated circuit according to claim 10, wherein

said storage circuit includes a semiconductor memory circuit for specifying data of a plurality of bits to be held, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ...,

VREFintn-1) is changed based on data of a plurality of bits stored in said semiconductor memory circuit.

12. The semiconductor integrated circuit according to claim 11, wherein

said storage circuit includes a register for specifying data of a plurality of bits to be held, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said register.

13. The semiconductor integrated circuit according to claim 1, further comprising a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and wherein

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

14. The semiconductor integrated circuit according to claim 13, further comprising a selection circuit for selecting said first storage circuit or said second storage circuit, and wherein

said relationship between said external reference

potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

15. The semiconductor integrated circuit according to claim 1, further comprising a selection circuit for selecting said first storage circuit or said second storage circuit, and wherein

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

16. The semiconductor integrated circuit according to claim 5, wherein said input circuit compares an input data signal with the reference potential having n-1 values at the timing of a clock signal's leading and trailing edge or either edge and outputs a comparison result.

17. The semiconductor integrated circuit according to claim 13, wherein said input circuit compares an input data signal with the reference potential having n-1 values at the timing of a clock signal's leading

and trailing edge or either edge and outputs a comparison result.

18. The semiconductor integrated circuit according to claim 14, wherein said input circuit compares an input data signal with the reference potential having n-1 values at the timing of a clock signal's leading and trailing edge or either edge and outputs a comparison result.

19. A semiconductor apparatus system, comprising:

a motherboard including an input/output terminal section and a data signal line and an external reference signal line connected to this input/output terminal section, and

a plurality of semiconductor integrated circuits which is mounted on said motherboard and includes a reference potential conversion circuit connected to said external reference signal line, supplied with n-1 (n is 2 or larger natural number) external reference potentials (VREF1, VREF2, ..., VREFn-1), and generating other potentials (VREFint1, VREFint2, ..., VREFintn-1) differing from said external reference potentials and further includes an input circuit supplied with output potentials (VREFint1, VREFint2, ..., VREFintn-1) from said reference potential conversion circuit as reference potentials, supplied with a data signal from said data signal line, comparing the input data signal with reference potentials having n-1 values for

determination, and generating a determination result.

20. The semiconductor apparatus system according to claim 19, wherein

said semiconductor integrated circuit further comprises a storage circuit for holding data of a plurality of bits, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said storage circuit.

21. The semiconductor apparatus system according to claim 19, wherein

said semiconductor integrated circuit further comprises a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

22. The semiconductor integrated circuit according to claim 19, wherein said semiconductor integrated circuit further comprises a selection circuit for selecting said first storage circuit or said second

storage circuit, and

said relationship between said external reference potentials (VREF1, VREF2, ..., VREFn-1) and said internal reference potentials (VREFint1, VREFint2, ..., VREFintn-1) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.